



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,925	03/25/2004	Hiroshi Yamazaki	1324.70190	6761

7590 06/11/2008
Patrick G. Burns, Esq.
GREER, BURNS & CRAIN, LTD.
Suite 2500
300 South Wacker Drive
Chicago, IL 60606

EXAMINER

NADKARNI, SARVESH J

ART UNIT	PAPER NUMBER
----------	--------------

2629

MAIL DATE	DELIVERY MODE
-----------	---------------

06/11/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/809,925	Applicant(s) YAMAZAKI, HIROSHI	
	Examiner SARVESH J. NADKARNI	Art Unit 2629	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 04/28/2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
- b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
- (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
- (b) ☐ They raise the issue of new matter (see NOTE below);
- (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
- (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See Continuation Sheet. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
- The status of the claim(s) is (or will be) as follows:
- Claim(s) allowed: _____.
- Claim(s) objected to: _____.
- Claim(s) rejected: 1-12.
- Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629

/Sarvesh J. Nadkarni/
Examiner, Art Unit 2629

Continuation of 3. NOTE: Claims 4 and 9 as amended will require further consideration and search. Claim 4 has been amended to include the limitation "terminals" and therefore will require at least further consideration and search. Claim 9 has been amended to include the limitations "a sampling memory that samples and stores said data signals received from the first and second data latch" which will require at least further search and consideration.

Applicant traverses the rejection of claim 11 as being anticipated by Go and argues that Go fails to disclose that "a timing controller displaces the phase between the data signals of the odd-number dots and the even number dots by 180 degrees". Examiner respectfully disagrees. As addressed in the Final Action, Go clearly discloses this limitation at least at column 6, lines 20-25. Furthermore, Examiner directs the Applicant to lines 20-64 further describing lines D1, D3, and D5 as odd data lines connected to first clock signal FD1, and D2, D4, and D6 as even data lines connected to FD2 wherein the phase of the signals applied to the odd and even data lines are 180-degrees apart. Therefore, claim 11 stands as rejected.

Applicant traverses the rejection of claims 1 and 5 as being unpatentable over Go in view of Misawa and argues that these two references do not disclose "a liquid crystal display device with first and second clock signal lines that are equipped in parallel and have a load capacitance that are equal or substantially equal by equipping the load means." Examiner respectfully disagrees. As addressed in the Final Action, Go in view of Misawa clearly teaches the limitation and as described by Applicant, lines 218 and 219 as described by Misawa have load capacitances that are substantially equal. The Misawa teaching although describing the lines crossing to keep equidistant from the video signal line, does not mention the lines intersect and therefore a twisting helical nature is presumed from the teaching to provide for normal functioning. Therefore, claims 1 and 5 stand rejected.

Regarding Applicant's argument that claim 1 encompasses the ability to adjust the load capacitance by the load means so as to have load capacitances that are equal or substantially equal. Examiner respectfully disagrees. The load means' adjustability has not been claimed in claim 1 and therefore this assertion has no basis. Therefore, claim 1 stands as rejected.

Applicant traverses the rejection of claim 7 as being unpatentable over Go in view of Jeon and argues that these two references fail to disclose "a selection signal that is used to select the first or second clock signal." Examiner respectfully disagrees. As clearly described in the Final Action, the combination of selection signal as taught by Jeon with the clock signal lines of Go would be obvious to one of ordinary skill in the art for the commonly understood benefits of reduction of external connection signals as taught by Jeon at column 2, lines 48-end. Therefore claim 7 stands as rejected.

Applicant traverses the rejection of claim 9 as being unpatentable over Go in view of Jeong and argues that the combination does not disclose "a sampling memory that samples and stores data signals". As described above, amended claim 9 will require further search and consideration.

Applicant traverses the rejection of claim 10 as being unpatentable over Go in view of Jeong and argues that the combination does not disclose "a selection signal which is used as the basis for selecting a first or second clock signal." Examiner respectfully disagrees. As indicated in the Final Action, Jeong clearly teaches the data latch and multiplexer as taught at column 4, lines 61-end and continued at column 5, lines 1-8. The device in combination with Go clearly would allow for selecting a first or second clock signal as described in the Final Action. Therefore, claim 10 stands as rejected.

Applicant traverses the rejection of claim as being unpatentable over Go in view of Ogata and argues that the combination does not disclose "a dot consists of a plurality of bits." Examiner respectfully disagrees. As clearly described in the Final Action, Ogata teaches a data signal having odd bits and another signal line having even bits. Therefore the data signal corresponds to the dot and the bits in Ogata are congruent to the bits in the current application. Applicant further argues that Go in view of Ogata does not disclose "the output pin for a bit of a color of an odd-number dot is adjacent to an output pin of the same bit of the same color of an even-number dot." Examiner respectfully disagrees. As described in the Final Action, Ogata clearly depicts the adjacency as claimed in claim 12 at least at the demonstrative FIG. 1 illustrating parallel odd lines adjacent to even lines. Therefore, claim 12 stands as rejected.